PQLab

PRIMARIUS

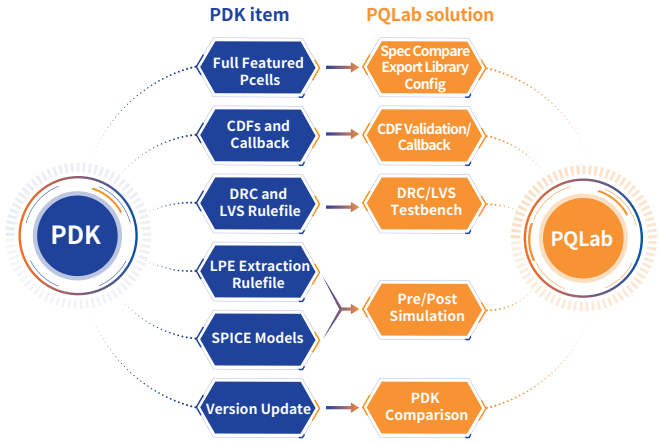
Advanced PDK Verification Platform

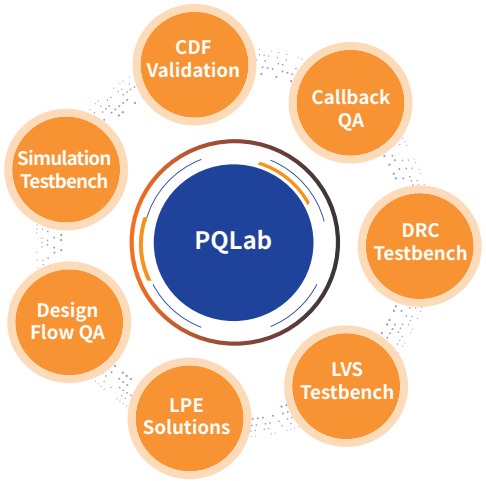
Introduction

PQLab is an advanced PDK (Process Design Kit) verification platform. As the semiconductor manufacturing technology continues scaling down to smaller geometries, PDK complexity increases rapidly. PDK validation becomes much more complicated than ever before, while taking more time.

Primarius has developed PQLab as a complete solution based on years of experiences in advanced PDK development and verification to address this challenge.

PQLab is an automated QA software for PDKs, featuring a multitude of qualification mechanisms of PDK integrity, including technology files, PCell CDF and PCell physical verification (DRC & LVS). PQLab supports PDK verification for planar process (0.18um to 22nm) and FinFET process (16nm to 5nm), covering applications in digital logic, analog, high voltage, and RF circuits. PQLab helps foundries' PDK engineers ensure PDK quality, enabling IC designers to easily analyze and qualify foundry PDKs and benchmark between different PDK versions and design flows.

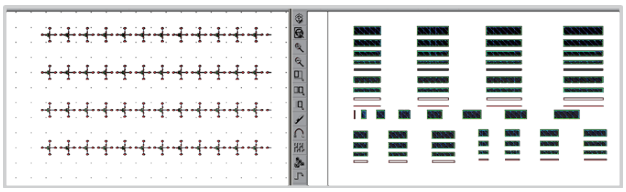




Key Advantages

- Versatility
  Supports the PDK format and EDA tools of mainstream Foundries
- Completeness
  - Supports PCell validation and different flows like Calibre LVS+
  - Full coverage of QA patterns with complete QA reports
  - Supports various combinations of different models, LVS, and PEX formats
- Automation
  Highly-integrated automation PDK QA environment
- Efficiency
  Built-in pattern generation module for each PDK component
- Flexibility
  Supports test pattern user customization
- Reusability
  The existing PDK QA setting could be re-used in a future project.

Specifications



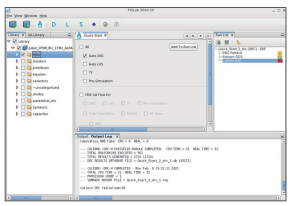
- Test pattern generation automation
  - Automatically generates the test patterns for DRC, LVS, CDF, and other PDK components
- Supports CDF verification
  - CDF Spec, CDF Callbacks, CDF Parameter and SPICE Model parameter consistency inspection
- Supports DRC/LVS verification
  - Intelligently auto-generates the minimal set of DRC and LVS inspection test patterns to ensure proper PDK functionality for all PCell parameter combinations.
- Supports comprehensive simulation
  - Ensure the PDK output consistency through automatic comparison between pre-layout and post-layout simulations
  - Supports comparison of the results from different combinations of the SPICE model, LVS and PE.
- Supports DC OP back-annotation function verification
- Supports PCell input variable function verification

Applications

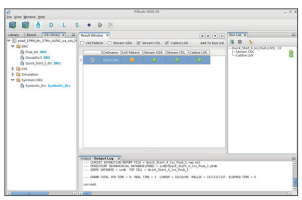
- Foundry PDK development and verification
- Fabless & IP vendor evaluation and verification of foundries' process

Application Examples

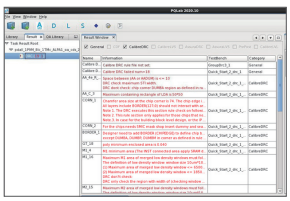
PDK QA Setting GUI



QA Library GUI



DRC QA Result



Comparison between pre-layout an post-layout simulation