# NanoSpice Giga

PRIMARIUS

Large Capacity & High Precision SPICE Simulator

Introduction

NanoSpice Giga is industry's Giga-scale SPICE simulator. Its innovative parallel simulation engine is built using big data architecture that effectively handles billion-element designs. This capability makes NanoSpice Giga ideal for verification and signoff of memory, custom or semi-custom digital circuits, and full-chip designs.

NanoSpice Giga is designed for accuracy verification and signoff of advanced memory designs. In this area, traditional FastSPICE has fundamental limitations. The pure SPICE engine of NanoSpice Giga offers significantly higher accuracy for power, leakage, timing/noise characterizations, and verification. NanoSpice Giga's superior parallelization technologies deliver faster simulation speed without sacrificing accuracy. NanoSpice Giga can be the golden signoff simulator for memory IP and full-chip verification with high precision and performance.
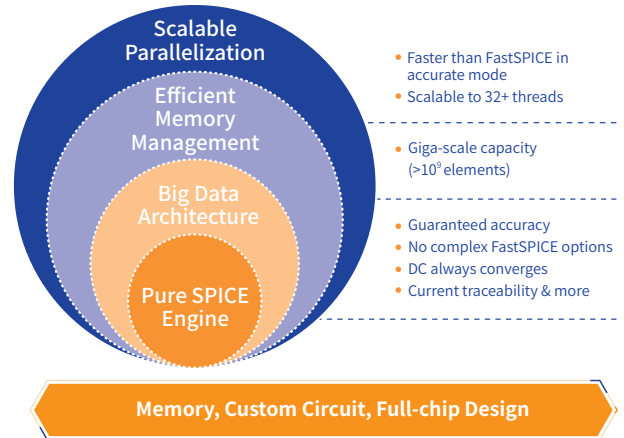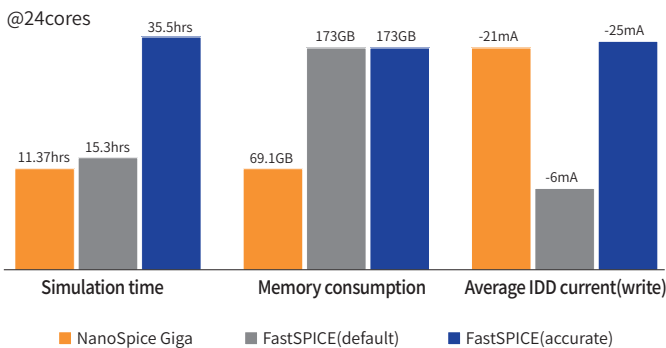
Key Advantages

- **Superior accuracy**
  Pure SPICE accuracy with DC converged
- **Giga-scale capacity**
  Ability to handle full-chip verification and signoff ($>10^9$ elements)
- **High performance**
  Scalable to 32+ threads, high performance parallelization. Special optimization for FinFET/FD-SOI processes
- **No need for complicated options**
  No tuning, directly replaces existing simulator
- **Foundry validated accuracy**
  16/14/7/5/3nm FinFET and 28nm FD-SOI ready

Application Examples

IDD verification of SRAM full-chip including 4.95E8 devices by NanoSpice Giga using default option settings.

Scalable Parallelization / Efficient Memory Management / Big Data Architecture / Pure SPICE Engine

- Faster than FastSPICE in accurate mode
- Scalable to 32+ threads
- Giga-scale capacity ($>10^9$ elements)
- Guaranteed accuracy
- No complex FastSPICE options
- DC always converges
- Current traceability & more

Memory, Custom Circuit, Full-chip Design

Type	Thread	Reference	NanoSpice Giga	Speedup
Pre-layout NOR Flash READ	8	3h	0.83h	3.6X
Pre-layout NOR Flash PROGRAM	8	38h	7h	5.42X
Pre-layout NOR Flash ERASE	8	24h	4h	6X
Post-layout NOR Flash READ	8	108h	35h	3.08X

Specifications

- Supports HSPICE and Spectre netlist formats
- Supports all public domain models, user-defined models
  - MOSFET: BSIM3, BSIM4, BSIM-BULK, BSIM-IMG, BSIM-CMG, BSIM-SOI, LETI-UTSOI, PSP, HiSIM2, HiSIM_HV, EKV3
  - BJT: MAXTRAM, VBIC, HICUM; TFT: a-Si TFT, poly-Si TFT
  - Diode: JUNCAP, JUNCAP200, DIODE_CMC; Varactor: MOSVAR
  - Resistor: R2_CMC, R3_CMC; HEMT: ASM-HEMT; JFET/MESFET; TMI/Custom PMI; Bsource
- Supports full SPICE analysis features
  - OP, DC, AC, Noise, Transient, Trannoise, FFT, Sweep, Alter, Bisection Stability, Pole-Zero, Monte Carlo, DC Match, AC Match
- Supports Verilog-A (LRM2.4) and behavioral sources
- Supports VEC and VCD stimulus files
- Supports standard output formats for data analysis: FSDB, PSFASCII, SPICEASCII, ASCII, etc
- Supports S-parameter, Transmission line (W-element, T-element), IBIS model
- Supports SPEF, DSPF, DPF back-annotation
- Support public cloud platform, hybrid cloud and private cloud

Applications

- Memory IC high accuracy verification (Flash, DRAM, SRAM, MRAM etc.)
- Panel (LCD/OLED) circuit high accuracy simulation and verification
- Large scale analog circuit post simulation and verification
- Full-chip SoC high accuracy simulation and verification