2025 中国研究生创“芯”大赛·EDA 精英挑战赛

一、赛题名称

应用 DTCO 方法学提升环形振荡电路的性能

二、命题单位

上海概伦电子股份有限公司

三、赛题背景

随着半导体工艺节点的持续演进和复杂度的不断提升，最大化工艺节点的收益已成为半导体行业的共识和核心挑战。在此背景下，设计工艺协同优化（DTCO）逐渐成为实现这一目标的关键技术路径。

在传统的半导体芯片设计中，设计工作通常是在既定的工艺和 PDK（工艺设计套件）框架下进行电路优化。然而，DTCO 则突破了这一局限，它从芯片的设计需求出发，探索在工艺层面的优化空间。随着摩尔定律的延续面临越来越大的挑战，开发和使用新一代半导体工艺的成本不断攀升，而新一代工艺带来的性能提升却逐渐收窄。在这种情况下，借助 DTCO 对半导体工艺和电路设计进行尽可能多的优化，尤其是在先进制程“断供”的背景下深度挖掘工艺潜能，正变得越来越重要。据半导体研究机构 IMEC 的分析，从 10 nm 工艺节点开始，DTCO 在半导体工艺节点演进中的作用逐步提升，并有望逐渐取代之前摩尔定律中单纯依靠减小工艺特征尺寸的模式。

四、赛题描述

环形振荡器是一种用于通信系统的电路，用于产生特定频率的时钟信号。它的工作原理是通过正反馈回路来实现自激振荡。具体来说，环形振荡器由一串相同的反相器组成，每级反相器的输出连接到下一级反相的输入。当输入信号经过放大器的放大

后，经过一系列的传递和反相，最终回到第一个放大器的输入端，形成一个闭环，从而产生振荡。环形振荡器在无线通信、射频电路和音频处理等领域有广泛的应用。

基于 55 nm 工艺节点(沟道长度 L_{ch}=55 nm, 栅氧化层厚度 T_{ox}= 1.5nm, V_{dd}=1.4 V) 进行 TCAD 仿真,完成 NMOS 和 PMOS 工艺仿真和器件仿真,产生建模所需的 IV/CV 数据，基于 BSIM4 器件模型进行模型参数提取，编写 51 级环形振荡器网表并使用提取的器件模型进行仿真，得到电路的**振荡频率**和**功耗值（静态，动态功耗）**，并以提升振荡频率和降低功耗为目标，指导工艺条件的调整，按以上流程迭代至提升目标。

- 任务 1、实现 55 nm 工艺节点 NMOS 和 PMOS 工艺仿真和器件仿真，完成配置并运行 TCAD 工具，并分析影响器件特定电学性能的工艺条件。
- 任务 2、基于 TCAD 仿真数据，选择 BSIM4 模型，完成直流和交流模型参数的提取。
  - 参考脚本驱动（自定义脚本格式）的提取流程，完成直流参数和交流参数提取
  - 模型拟合精度，精度需满足以下条件:

SPEC	拟合精度要求
$\mathbf{C_{gg\_inv}}$	≤3%
$\mathbf{C_{gg\_0}}$	≤3%
$\mathbf{V_{tlin}}$	≤30mv
$\mathbf{V_{tsat}}$	≤30mv
$\mathbf{V_{tgm}}$	≤50mv
$\mathbf{I_{dlin}(V_{gs}=V_{dd}, V_{ds}=0.05V)}$	≤3%

$I_{dsat}(V_{gs}=V_{dd}, V_{ds}=V_{dd})$	≤3%
$I_{d1}(V_{gs}=V_{dd}, V_{ds}=V_{dd})$	≤5%
$I_{d2}(V_{gs}=0.5*V_{dd}, V_{ds}=V_{dd})$	≤10%
$I_{d3}(V_{gs}=V_{dd}, V_{ds}=0.25V_{dd})$	≤5%
I_{off}	≤30%

- 任务 3、完成环形振荡器的网表编写和仿真，提取振荡频率和静态功耗、动态功耗。
- 任务 4、根据仿真结果，调整器件工艺参数：FabTCAD 可调节的工艺条件，离子注入的 species、waferDose、energy 参数；扩散的 time、temperature、finalTemperature 参数，驱动上面的 TCAD 仿真-模型参数提取-电路仿真过程，直至达到提升目标。

五、评分标准

1. 必答题：任务 1-3

完成此 RO 电路的 DTCO 正向流程，包括工艺仿真、器件仿真，器件模型参数提取，RO 电路仿真和振荡频率和静态、动态功耗的提取 （15 分）。

其中：

任务 1：工艺仿真、器件仿真（2 分）

任务 2：器件模型参数提取，并满足所有拟合精度要求。不满足不得分（8 分）

任务 3：RO 电路仿真和振荡频率和静态、动态功耗的提取 （5 分）

2. 任务 4：完成完整迭代流程，实现设计指标的提升（0.2%以上）得 15 分。各参赛队按设计指标提升幅度（相对值%）的综合排名可额外加分。排名前 10%加 15 分，10%-20%加 13 分，20%-30%加 11 分，30%-40%加 9 分，40%-50%加 7 分，50%-60%加 5 分，60%-70%加 3 分，排名在 70% 之后不加分。（总计 30 分）

3. 任务 4 加分题：完成上述流程迭代消耗的仿真时间越短，加分越高。排名前 20%加 5 分，20%-40%加 3 分，40%-60%加 1 分，排名在 60% 之后不加分。（+5 分）

4. 附加题：引入优化算法实现 DTCO 流程中关键步骤的自动化并实现最终目标优化，如

a) 引入神经网络或机器学习算法，替代或加速 TCAD 的工艺仿真和器件仿真流程。要求在相同的工艺条件下，相对于传统 TCAD 仿真，基于神经网络或机器学习算法的 TCAD 仿真 IV 和 CV 仿真结果 RMS 误差小于 3%，仿真时间缩短至少 50%。

计算 RMS 的表达式如下所示，

$$\mathrm{RMS}_{\mathrm{maxY}} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left(\frac{Tar_i - Ref_i}{max_{1\le i\le n}(Ref_i)}\right)^2}$$

其中 n 表示数据点的个数，Tar 表示 Target 数据，Ref 表示 Reference 数据。基于神经网络或机器学习算法的 TCAD 仿真结果作为 Target 数据，传统 TCAD 仿真结果作为 Reference 数据。

参赛队伍根据排名得分，名次每降低一位，得分减少 2 分。第一名 10 分，第二名 8 分，第三名 6 分，后续名次得分按此规则递减。（+10 分）

b) 参考脚本驱动的参数提取优化算法，自定义参数提取优化算法实现提取速度的提升。优化后 IV 曲线 RMS 误差小于 5%，Idlin、Idsat RMS 误差小于 3%。优化后的参数提取算法比参考算法用时更短，时间缩短 50%以上可得分。参赛队伍根据排名得分，名次每降低一位，得分减少 2 分。第一名 10 分，第二名 8 分，第三名 6 分，后续名次得分按此规则递减。（+10 分）

六、参考资料

概伦电子 FabTCAD 是一款建立在半导体物理基础之上的有限元仿真工具，配合自研网格划分引擎，从物理底层出发求解工艺模型和器件物理模型的偏微分方程。用户可以根据半导体加工中的各个步骤的工艺条件，使用 FabTCAD 中的工艺模型建立虚拟 FAB 仿真流程，得到器件结构和掺杂分布。用户从器件结构和掺杂分布出发，耦合不同的器件物理模型，可得到器件的电学特性。

MeQLab 是一款跨平台建模软件，提供完整的器件模型提取方案。该软件集成丰富的射频建模应用模板，同时开放脚本编程环境，支持用户自定义设置如去嵌程序、模型自动提参流程设计等应用，满足硅基或者化合物工艺器件建模应用。

NanoSpice X 是概伦电子推出的高精度 SPICE 仿真器，凭借并行仿真技术、自适应 SPICE 引擎、矩阵求解技术、后仿电路拓扑优化和 RC 约简技术，可支持亿级器件规模的电路仿真，并保持 SPICE 级精度。其自适应 SPICE 引擎可根据用户指定的电路类型，自动匹配工作原理、电路结构、电路频率等方面最适用的仿真算法，同时支持通用模拟仿真选项以满足非定制用户需求。

七、补充

流程时间和资源评估：正向完成工艺和器件仿真、模型参数提取需要 5~8 小时，包括：

1. 工艺仿真和器件仿真(测试机器硬件信息：CPU:24 核 32 线程、13th Gen Intel® Core™ i9-13900K、主频 3GHZ。内存：32G*4），跑一组工艺仿真耗时 30 分钟到 2 小时不等，跑一组器件仿真（I_d_V_g+I_d_V_d+C_V）耗时 10 分钟到 1 小时不等，若出现不收敛的情况耗时会增加；

2. 模型参数手动提取 2-2.5 小时；

3. 驱动仿真和查看和分析结果约 0.5 小时。

FabTCAD 运行环境：CentOS 7.9 或 CentOS 8 以上；推荐硬件配置：Intel 64 位 CPU，主频 2.6G 及以上，运行内存大于 32G。

*本赛题指南未尽问题，见赛题 Q&A 文件

2025 China Postgraduate IC Innovation Competition·EDA Elite Challenge Contest

1. Problem

Applying DTCO Methodology to Enhance Ring Oscillator Circuit Performance

2. Company

Shanghai Primarius Technologies Co., Ltd.

3. Problem Background

With the continuous evolution of semiconductor process nodes and the ever-increasing complexity, maximizing the returns from each process node has become a shared understanding and central challenge within the semiconductor industry. In this context, Design Technology Co-Optimization (DTCO) has gradually emerged as a key pathway to achieve this goal.

In traditional chip design, it is typically conducted under fixed process parameters and within the constraints of the PDK (Process Design Kits) to achieve circuit optimization. However, DTCO breaks through this limitation, it adopts a design-driven approach to identify optimization potential at the process level. The continuation of Moore's Law is facing increasingly greater challenges, the costs associated with developing and adopting new-generation semiconductor processes continue to climb, while the performance gains delivered by these advanced processes are gradually narrowing. In this case, it is becoming increasingly critical to leverage DTCO to maximize optimization of semiconductor processes and circuit design, especially maximizing process potential amid supply chain

disruptions affecting advanced nodes. According to analysis by IMEC, starting from the 10 nm process node, DTCO has been playing an increasingly vital role in semiconductor process node advancement, and it is projected to gradually replace the traditional Moore's Law paradigm that relied exclusively on process feature size scaling.

4. Problem Description

Ring oscillator is a circuit commonly employed in communication systems for generating clock signals at specific frequencies. Its operational mechanism achieves self-sustaining oscillation through a positive feedback loop. Specifically, ring oscillator is constructed as a cascade of identical inverters, where the output of each inverter is directly connected to the input of the subsequent stage. When an input signal is amplified and undergoes sequential propagation with phase inversion through the amplifier chain, it ultimately loops back to the input of the initial amplifier, forming a closed loop that enables self-reinforcing oscillation. Ring oscillators find a wide range of applications in fields such as wireless communications, RF circuits, and audio processing.

Based on a 55 nm process node (channel length L_{ch} = 55 nm, gate oxide thickness T_{ox} = 1.5 nm, V_{dd} = 1.4 V), TCAD simulations are performed to conduct both process and device simulations for NMOS and PMOS transistors, generating IV/CV datasets required for modeling. Following BSIM4 model parameter extraction, a 51-stage ring oscillator netlist is authored and simulated using the extracted device models to measure oscillation frequency along with static and dynamic power consumption. This iterative refinement process targets frequency enhancement and power reduction by adjustments to process conditions until the optimal results are achieved.

- Task 1: Performing process and device simulations for 55 nm NMOS/PMOS transistors require configuring and executing TCAD tools to analyze how process conditions influence targeted electrical characteristics.
- Task 2: Based on TCAD simulation data, the BSIM4 model is selected to perform comprehensive extraction of both DC and AC model parameters.
  - Referencing the extraction workflow of script-driven (custom script format) to complete DC and AC parameter extraction
  - Model fitting accuracy must satisfy the following conditions:

SPEC	拟合精度要求
C_{gg_inv}	≤3%
C_{gg_0}	≤3%
V_{tlin}	≤30mv
V_{tsat}	≤30mv
V_{tgm}	≤50mv
$I_{dlin}(V_{gs}=V_{dd}, V_{ds}=0.05V)$	≤3%
$I_{dsat}(V_{gs}=V_{dd}, V_{ds}=V_{dd})$	≤3%
$I_{d1}(V_{gs}=V_{dd}, V_{ds}=V_{dd})$	≤5%
$I_{d2}(V_{gs}=0.5*V_{dd}, V_{ds}=V_{dd})$	≤10%
$I_{d3}(V_{gs}=V_{dd}, V_{ds}=0.25V_{dd})$	≤5%
I_{off}	≤30%

- Task 3: Complete netlist generation and simulation of the ring oscillator to extract oscillation frequency, static power, and dynamic power.

- Task 4: Adjust device process parameters based on simulation results: Iteratively drive the TCAD simulation → model parameter extraction → circuit simulation workflow by tuning FabTCAD adjustable process conditions — including ion implantation (species, waferDose, energy) and Diffusion (time, temperature, final Temperature)— until target specifications are achieved.

5. Scoring Criteria

5.1 Required questions: Task 1~3

Complete this DTCO flow for the RO circuit, including process simulation, device simulation, model parameter extraction, RO circuit simulation, and extraction of oscillation frequency, static power, and dynamic power (15 points), where:

Task 1: Process simulation, device simulation (2 points)

Task 2: Device model parameter extraction. Device parameter extraction shall meet all accuracy specs. Non-conformance yields zero credit (8 points)

Task 3: RO circuit simulation and extraction of oscillation frequency, static and dynamic power consumption (5 points)

5.2 Task 4: Complete full process iteration to achieve improvement（more than 0.2%）in design metrics (15 base points). Additional bonus points correlate directly with improvement percentile rankings: top 10% scores 15 points, 10%–20% scores 13 points, 20%–30% scores 11 points, 30%–40% scores 9 points, 40%–50% scores 7 points, 50%–60% scores 5 points, and 60%–70% scores 3 points, whereas rankings below 70% receive no points. The maximum achievable bonus is 15 points. (30 points)

5.3 Task 4 bonus question: The shorter the time consumed to complete the process iteration,

the higher the bonus achieved, specifically: Top 20% scores 5 points; 20% – 40% scores 3 points; 40% – 60% scores 1 points; those beyond top 60% receive no points. (+5 points)

5.4 Bonus questions: Introducing optimization algorithms to automate key steps in the DTCO process. For example,

a) Introduce neural networks or machine learning algorithms to replace or at least accelerate TCAD process and device simulation workflows. Under identical process conditions, TCAD simulations based on neural network or machine learning algorithms achieve an RMS error of less than 3% compared to traditional TCAD IV/CV simulation results, while reducing simulation time by at least 50%. The RMS formula is as below,

$$\mathrm{RMS}_{\mathrm{maxY}} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}\left(\frac{Tar_i - Ref_i}{max_{1\le i\le n}(Ref_i)}\right)^2}$$

where n denotes the number of data points, Tar represents the Target data, and Ref represents the Reference data. The TCAD simulation results based on neural network or machine learning algorithms serve as the Target data, while the conventional TCAD simulation results serve as Reference data. Teams are ranked with 2-point decrements per rank down, starting from 10 points for 1st place (e.g., 2nd=8 points, 3rd=6 points). (+10 points)

b) Develop a custom parameter extraction optimization algorithm to surpass the benchmark script-driven approach in extraction speed. The optimized solution must achieve: IV curve RMS error < 5%; Idlin/Idsat RMS error < 3%; and ⩾50% time

reduction versus reference algorithm to qualify for scoring. Teams are ranked with 2-point decrements per rank down, starting from 10 points for 1st place (e.g., 2nd=8 points, 3rd=6 points). (+10 points)

6. Reference materials

Primarius FabTCAD is a finite element simulation tool built upon semiconductor physics fundamentals. Cooperate with self-developed grid generation engine, it solves partial differential equations for both process models and device physics models. Users can establish a virtual fabrication flow using process models in FabTCAD by defining process conditions for each semiconductor manufacturing step, thereby deriving device structures and doping profiles. Starting from device structures and doping profiles, users can derive electrical characteristics by coupling different device physics models.

MeQLab is a cross-platform modeling software that delivers a comprehensive solution for device model extraction. The software integrates a comprehensive suite of RF modeling application templates while providing an open scripting environment, enabling user-customized configurations — such as de-embedding procedures and automated parameter extraction workflow design—to accommodate device modeling applications for both silicon-based and compound semiconductor technologies.

NanoSpice X is a high-precision SPICE simulator developed by Primarius Technologies. With its parallel simulation technology, adaptive SPICE engine, matrix solving techniques, post-layout topology optimization, and RC reduction technology, it supports the simulation of large-scale circuits with over millions of components while maintaining SPICE accuracy. Its adaptive SPICE engine automatically matches the most suitable simulation algorithms

based on user-specified circuit types—considering operating principles, circuit structures, and operating frequencies, while also supporting general analog simulation options to meet the needs of conventional users.

7. Supplement

Process time and resource assessment: Completing process/device simulation and model parameter extraction in a forward design flow requires 5 to 8 hours. Including:

7.1 Process and device simulations were executed on a test system equipped with a 24-core/32-thread 13th Gen Intel® Core™ i9-13900K CPU @ 3.0 GHz and 128 GB RAM (32GB*4). One set of process simulations required between 30 minutes and 2 hours per run, while a set of device simulations (I_d_V_g+I_d_V_d+C_V) took 10 minutes to 1 hour. Runtime could increase significantly when addressing non-convergence issues.

7.2 Manual extraction of model parameters takes 2-2.5 hours.

7.3 It takes about 0.5 hours to drive the simulation, view, and analyze the results.

FabTCAD Operating Environment: CentOS 7.9 or CentOS 8+. Recommended Hardware Configuration: Intel 64-bit CPU 2.6 GHz or higher, with RAM exceeding 32 GB.

*For questions not covered in this guide, please refer to the Q&A document